Low Power, Low Noise Ultrasound Receive Front-End Eight-Channels of LNA, VGA, AAF, CPS & 12-Bit, 50MHz ADCs

Features

- 1.8V Analog/Digital supply
- 3.3V supply for CW Doppler output bias
- Fully differential inputs and outputs
- SPI programmable LNA gain = 14dB/18dB
- LNA input range $480mV_{PP}/300mV_{PP}$
- Dual mode active input impedance matching
- 1.1nV/√Hz Input Voltage Noise at 5.0MHz
- 1.0pA/√Hz Input Current Noise at 5.0MHz
- 0 to -47dB Linear-in-dB variable Gain of VCA
- 4 PGA Gain settings: 23.5, 29.0, 34.5 & 40.0dB
- Third Order Anti-Aliasing Filter (AAF)
- Program/Auto-tracking AAF (6.6~15MHz)
- Integrated 8×8 Cross-Point Switch (CPS)
- SNR 66dB, SFDR 74dB for ADC
- Built-in reference voltage
- LVDS per ANSI-644
- Fast overload recovery time
- Low power 95mW/ch, 50mW/ch CW

Applications

- Medical ultrasound imaging
- Portable ultrasound instrumentation
- Transducer signal processing

General Description

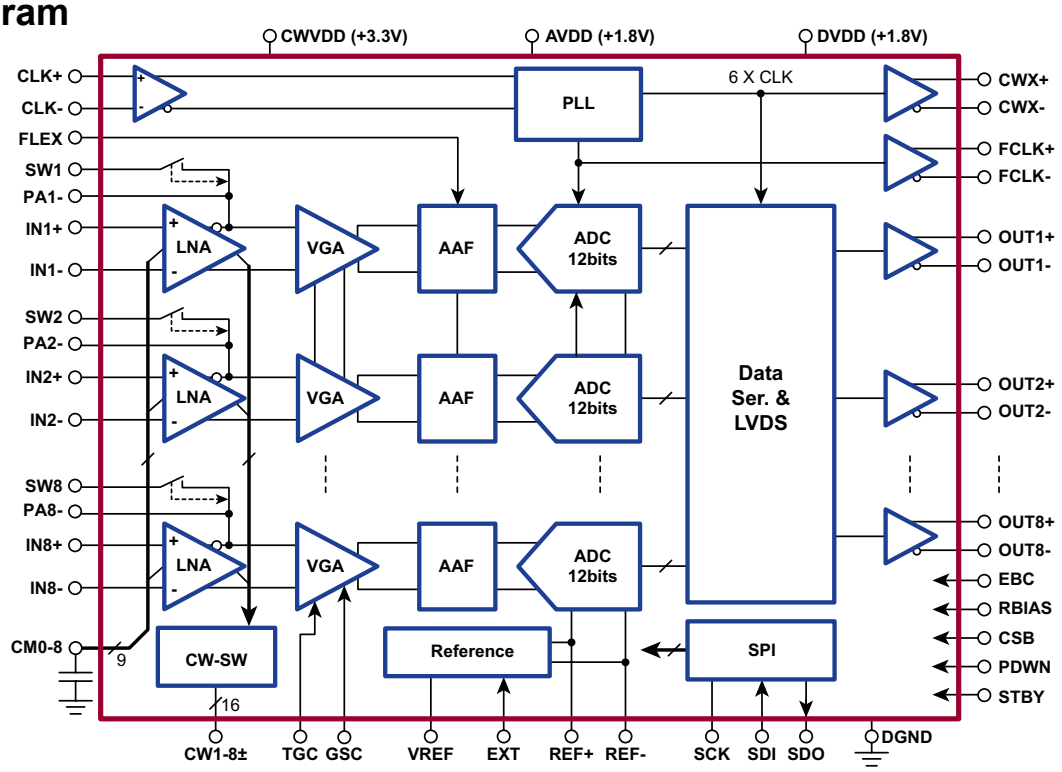
The MD3872 is an eight-channel front-end receiver for medical ultrasound imaging. Its excellent low power dynamic performance is especially suitable for portable ultrasound applications.

The circuit of each channel is composed of a 14dB/18dB low noise pre-amplifier (LNA), a voltage- controlled attenuator (VCA or TGC), a programmable gain amplifier (PGA), an anti-aliasing filter (AAF) and an analog-to-digital (ADC) converter. The gain and gain range of the VGA can be digitally configured separately. The gain of the PGA can be set to one of four discrete values: 23.5dB, 29dB, 34.5dB or 40dB. The VCA can be continuously varied by a control voltage from -47dB to a maximum of 0dB.

In CW mode, an integrated trans-conductance amplifier is driven by the LNA to generate differential output current. The resulting signal currents of each channel then connect to an 8×8 differential cross-point switch which can be programmed through the SPI.

The 12-bit ADC is based on a pipeline structure to provide high static linearity. The data, clock, and frame alignment signal outputs are serial LVDS in binary format for each channel.

Block Diagram



Ordering Information

Part Number	Package Option	Packing
MD3872HF-G	128-Lead TQFP (w/Heat Slug)	90/Tray

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
AV_{DD}, Positive supply	-0.3V to +2.0V
DV_{DD}, Positive supply	-0.3V to +2.0V
CWV_{DD}, Positive supply	-0.3V to +3.75V
V_{IN}, Any input pin voltage range	-0.3V to AV_{DD}
Storage temperature	-65°C to +150°C
Operating temperature	0°C to +70°C

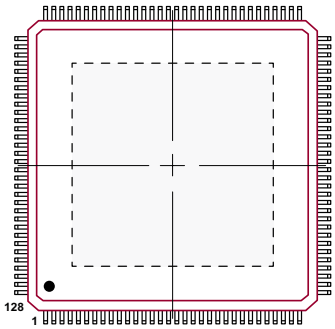
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Typical Thermal Resistance

Package	θ_{ja}
128-Lead TQFP	21°C/W*

** 4"x3", 4-layer 1oz 16-via PCB*

Pin Configuration



128-Lead TQFP
(top view)

Package Marking

Top Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin
A = Assembler ID
_____ = "Green" Packaging

Package may or may not include the following marks: Si or

128-Lead TQFP

Operating Supply Voltages

(Over operating conditions unless otherwise specified, $AV_{DD} = DV_{DD} = PV_{DD} = 1.8V$, $CWV_{DD} = +3.3V$, R_{SEL} = Hi, $R_S = 50\Omega$, $T_A = 25°C$)

Sym	Parameter	Min	Typ	Max	Units	Conditions
AV_{DD}	Analog circuit supply voltage	1.71	1.8	1.89	V	---
DV_{DD}	Digital circuit supply voltage	1.71	1.8	1.89	V	f_S = 40MHz
		1.80	1.90	1.98		f_S = 50MHz
CWV_{DD}	CW switch supply voltage	3.14	3.3	3.47	V	---
I_{AVDD}	AVDD per-chip	-	360	-	mA	---
	CWD mode	-	190	-		
I_{DVDD}	DVDD supply current	-	70	100	mA	f_S = 40MHz
		-	94	140		f_S = 50MHz
I_{CVDD}	CVDD supply current	-	0.80	1.0	mA	8-channel total
Power	Per-channel at 40MSPS	-	95	-	mW	---
	Per-channel at CW mode	-	50	-		
	Power-down	-	-	1.0		8-channel total
	Standby	-	100	-		

Low Noise Preamplifier

(Over operating conditions unless otherwise specified, $AV_{DD} = DV_{DD} = 1.8V$, $CWV_{DD} = +3.3V$, $G_{LNA} = 18dB$, $T_A = 25°C$)

Sym	Parameter	Min	Typ	Max	Units	Conditions
G_{LNA}	Pre-amplifier gain	-	14/18	-	dB	Selectable
R_{IN}	Input resistance	-	15	-	kΩ	Without active termination
C_{IN}	Input capacitance	-	10	-	pF	Without active termination
I_{BIAS}	Input bias current	-	1.0	-	nA	From ESD leakage
V_{IN}	Input voltage range	-	±240	-	mV	$GAIN_{LNA} = 1$
		-	±150	-		$GAIN_{LNA} = 0$
$V_{LNA-NOISE}$	Input voltage noise, 5MHz	-	1.3	-	nV/√Hz	LNA Gain of 14dB
		-	1.1	-		LNA Gain of 18dB
$I_{IN-NOISE}$	Input current noise	-	1.05	-	pA/√Hz	Without active termination
NF	Noise figure	-	4.4	-	dB	f = 5.0MHz, without active termination
		-	6.0	-		$R_S = R_{IN} = 50Ω$, f = 5.0MHz with active termination
BW	LNA -3dB bandwidth	-	65	-	MHz	Small signal bandwidth

Overall Channel Characteristics

((Over operating conditions unless otherwise specified, $AV_{DD} = DV_{DD} = 1.8V$, $CWV_{DD} = +3.3V$, R_{SEL} = Hi, $R_S = 50Ω$, $T_A = 25°C$)

Gain	Whole channel gain	-	58	-	dB	Without active termination, max. gain
$V_{CH-NOISE}$	Input voltage noise, 5.0MHz	-	2.0/1.5	-	nV/√Hz	LNA gain of 14 or 18dB
SFDR	Spurious-free dynamic range, -1dBFS, 5MHz	-	63.2	-	dBc	40Msps
		-	62.1	-		50Msps
SNRFS	Signal to noise ratio at full scale, -1dBFS, 5MHz	-	56.3	-	dBc	40Msps
		-	56.2	-		50Msps
HD2	Second harmonic distortion, -1dBFS, 5MHz, 40dB gain	-	-72	-	dBc	40Msps
		-	-68	-		50Msps
HD3	Third harmonic distortion, -1dBFS, 5MHz, 40dB gain	-	-63	-	dBc	40Msps
		-	-62	-		50Msps
IMD	IMD, two-tone	-	-63	-	dBc	f1 = 5.0MHz , f2 = 6.0MHz, at -7.0dBFS, 40dB gain
CSTK	Crosstalk	-	-70	-	dB	1.0MHz, $1V_{PP}$ at adjacent channel
Δt_{gd}	Group delay variation	-	±2.0	-	ns	2.0 to 10MHz, max gain range
t_{OLR}	Overload recovery time	-	5.0	-	ns	8dB gain, V_{IN} 10MHz $10mV_{PP}$ to $0.5V_{PP}$ step
f_{CHP}	High-pass cutoff frequency	-	50	-	kHz	---

Gain Control and Accuracy

(Over operating conditions unless otherwise specified, $AV_{DD} = DV_{DD} = 1.8V$, $CWV_{DD} = +3.3V$, R_{SEL} = Hi, $R_S = 50\Omega$, $T_A = 25°C$)

Sym	Parameter	Min	Typ	Max	Units	Conditions
V_{TGC}	Gain control voltage	0	-	1.8	V	Linear in dB, see Gain scaling diagram
V_{GSC}	Gain slope voltage	1.44	-	1.8	V	~62dB/V at 1.44V and 47.5dB/V at 1.8V
G_{RANGE}	Gain range	-	46.5	-	dB	GSC = 0 to +1.8V
G_{SLP}	Gain slope	-	47.5	-	dB/V	GSC = +1.8V
G_{MAT}	Ch. to ch. Gain matching	-	±1.5	-	dB	$0.4 < V_{TGC} < 1.2V$
E_{GAIN}	Gain error	-1.6	±0.5	+1.6	dB	
V_{OS}	Output offset voltage	-	15	-	LSB	EXT = Lo (internal reference)
R_{GSC}	Input resistance of GSC	-	90	-	kΩ	VTGC = 0V
I_{TGC}	Input current of TGC	-2.0	-	+2.0	µA	For the control range of 0V to 1.8V
td_{TGC}	Response time	-	500	-	ns	0 to 90% full Gain change

Logic Inputs Characteristics

(Over operating conditions unless otherwise specified, $AV_{DD} = DV_{DD} = 1.8V$, $CWV_{DD} = +3.3V$, R_{SEL} = Hi, $R_S = 50\Omega$, $T_A = 25°C$)

V_{IH}	High-level input voltage	$0.8V_{DD}$	-	-	V	---
V_{IL}	Low-level input voltage	-	-	$0.2V_{DD}$	V	---
I_{IH}	High-level input current	-	1.0	-	µA	---
I_{IL}	Low-level input current	-	1.0	-	µA	---
V_{OH}	High-level output voltage (I_{OH} = 0.5mA)	-	1.79	-	V	---
V_{OL}	Low-level output voltage (I_{OL} = 0.5mA)	-	0.05	-	V	---
C_{IN}	Input capacitance	-	2.0	-	pF	---

LVDS DC and Timing Characteristics

(Over operating conditions unless otherwise specified, $AV_{DD} = DV_{DD} = 1.8V$, $CWV_{DD} = +3.3V$, R_{SEL} = Hi, $R_S = 50\Omega$, $T_A = 25°C$)

V_{DO}	Differential output voltage	250	-	450	mV	---
V_{OCOM}	Output common-mode voltage	1.13	-	1.37	V	---
R_{TERM}	LVDS termination resistor	-	100	-	Ω	---
t_R	Rise time (20 % to 80 %)	-	800	-	ps	---
t_F	Fall time (80 % to 20 %)	-	800	-	ps	---
t_{DCLKWH}	DCLK output width high	-	4.1	-	ns	F_S = 40Msps
t_{DCLKWL}	DCLK output width low	-	4.1	-		
t_{D2D}	Data valid to DCLK rise/fall	-	$t_S/24$	-		
t_{F2D}	FCLK rise to DCLK rise	-	$t_S/24$	-		
t_{C2F}	CLK rise to FCLK rise	-	$t_S/2 + t_{PRP}$	-		

Internal and External Reference Characteristics

(Over operating conditions unless otherwise specified, $AV_{DD} = DV_{DD} = 1.8V$, $CWV_{DD} = +3.3V$, R_{SEL} = Hi, $R_S = 50\Omega$, $T_A = 25°C$)

Sym	Parameter	Min	Typ	Max	Unit	Conditions
V_{REF+}	ADC reference top voltage	-	1.4	-	V	ADC reference voltages, decoupling capacitors required
V_{REF-}	ADC reference bottom voltage	-	0.4	-	V	
V_{REF_EXT}	External reference voltage	-	1.0	-	V	EXT = Hi (select external V_{REF})
I_{REF_MAX}	Max reference output current	-	1.0	-	mA	---

CW Doppler Mode Characteristics

(Over operating conditions unless otherwise specified, $AV_{DD} = DV_{DD} = 1.8V$, $CWV_{DD} = +3.3V$, R_{SEL} = Hi, $R_S = 50\Omega$, $T_A = 25°C$)

g_m	Transconductance	-	9.5/15.2	-	mA/V	LNA Gain = 14/18dB
V_{COMM}	Common-mode voltage	1.5	-	3.6	V	CW Doppler output pins
$V_{CW\text{-}NOISE}$	Input-referred noise voltage	-	1.75/1.45	-	$nV/\sqrt{Hz}$	LNA Gain 14/18dB, $R_S = 0$, $R_{FB} = \infty$
$I_{OUT\text{-}BIAS}$	Output DC bias	-	2.8	-	mA	Per channel
$I_{OUT\text{-}SWING}$	Maximum output swing	-	±2.3	-	$mA_{P\text{-}P}$	---

Switching AC Characteristics

(Over operating conditions unless otherwise specified, $AV_{DD} = DV_{DD} = 1.8V$, $CWV_{DD} = +3.3V$, R_{SEL} = Hi, $R_S = 50\Omega$, $T_A = 25°C$)

F_S	ADC conversion rate	20	-	50	MSPS	---
t_S	Clock period	20	-	50	ns	---
t_{CLKWH}	Clock pulse-width high	-	12.5	-	ns	---
t_{CLKWL}	Clock pulse-width low	-	12.5	-	ns	---
t_{PRP}	ADC clock propagation delay	-	2.6	-	ns	---
PL_d	Pipeline latency delay	-	5.5	-	cycle	---
t_{SBY_DWN}	Time to standby	-	1.0	-	µs	---
t_{SBY_WUP}	Time to wakeup	-	10	-	µs	---
t_{PD_DWN}	Time to power down	-	1.0	-	µs	---
t_{PD_UP}	Time to power up	-	10	-	ms	---
t_1	SDI valid to SCK setup time	0	2.0	-	ns	See serial interface timing diagram
t_2	SDI valid to SCK hold time	4.0	-	-		
t_3	SCK high time	9.0	10	-		
t_4	SCK low time	9.0	10	-		
t_5	CSB pulse width	9.0	10	-		
t_6	SCK high to CSB low	-	4.5	-		
f_{SCK}	Serial clock max frequency	50	-	-	MHz	---

12-Bit ADC Digital Output Coding Table

Level	ADC Input Voltage	Binary Digital Output	Notes
4094	V_{IN} > +0.999756V	1111 1111 1110	---
...	...	...	---
2048	+0.000244V < V_{IN} < +0.000732V	1000 0000 0000	---
2047	-0.000244V < V_{IN} < +0.000244V	0111 1111 1111	---
...	...	...	---
0	V_{IN} < -0.999756V	0000 0000 0000	---

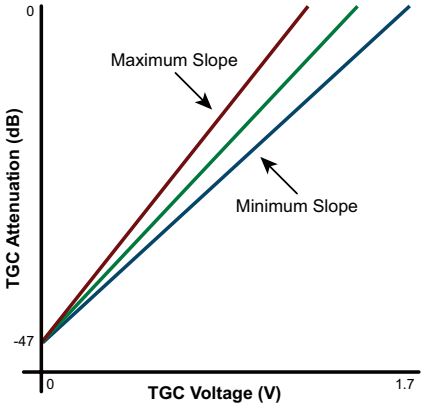
SPI Registers Address and Data Table

MSB (shift in first)	SPI Register Data Word											LSB
ADDR[3:0] Hex	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	-	STEP[2:0] (Alignment Step Size)			OUTDLY[5:0] (All channel OUTLVDS alignment delay setting)						ATP[1:0]	
1	TPD1[11:0] (LVDS Testing Pattern #1)											
2	CW1[5:0] (Channel 1 CW mode control)						CW2[5:0] (Channel 2 CW mode control)					
3	CW3[5:0] (Channel 3 CW mode control)						CW4[5:0] (Channel 4 CW mode control)					
4	CW5[5:0] (Channel 5 CW mode control)						CW6[5:0] (Channel 6 CW mode control)					
5	CW7[5:0] (Channel 7 CW mode control)						CW8[5:0] (Channel 8 CW mode control)					
6	-	-	-	CW/ TGC	CHOFF[7:0] (TGC Per Channel Power Off, 0=ON 1=OFF)							
7	-	-	AAF[1:0]		-	PDC	FLEX	-	SWLNA	GAIN-LNA	PG[1:0]	
8	-	-	CTL	PR[5:2]				-	AAF[5:2]			
9	-	-	-	-	ADCPD[7:0] (ADC Per Channel Power Down, 0 = ON 1 = OFF)							
A	-	-	-	-	Reserved Default all 0							
B	SWING[2:0]			-	Reserved Default all 0							
C	TPDC[11:0] (LVDS Testing Pattern #C)											
D	FDDLY[5:0] (FCLK and DCLK alignment delay setting)						-	-	-	-	-	-
E	Reserved Default all 0											
F	ADDR[3:0] to READ Back				-	-	-	-	-	-	-	-

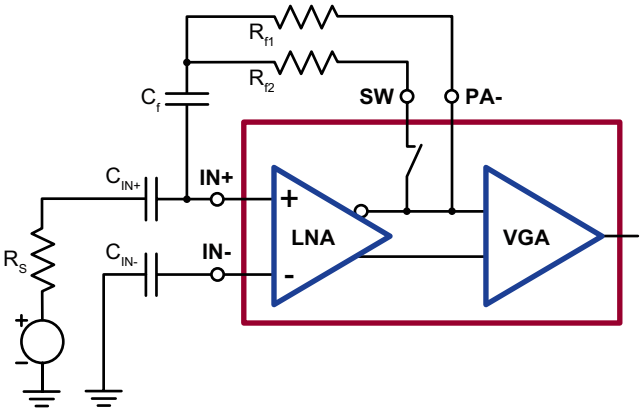
Note:

A bit marked as "-" means do-not-care whether it is set to "1" or "0".

TGC and GSC Voltage for Gain Scaling



LNA Feedback Configurations



ADDR=0 D[10:8]

STEP[2:0] LVDS Delay Step Size Control Table

STEP[2:0]	Delay Time Step Size	
000	100% (Default value)	120ps
001	133%	160ps
010	200%	240ps
011	400%	480ps
100	50% (min)	60ps
101	57%	69ps
110	67%	80ps
111	80%	96ps

Note:

1. *LDVS delay time step size control. Each bit will change the delay step size by 120ps. Setting a different value than 00 will change the DLOUT[5:0] and FDDLY[5:0] delay-time's step-size.*
2. *If f_s = 50MHz it is suggested that you use the minimum STEP[2:0] = 100.*

ADDR=0 D[7:2]

OUTDLY[5:0] LVDS ADC Data Output Delay Adjustment Table

OUTDLY[5:0]	Typical Rise Time Delay (ps)	Typical Fall Time Delay (ps)
00 0000	655	685
00 0001	766	805
… …	DELAY = 139.4 x FDDLY +655	DELAY = 148.5 x FDDLY + 699
11 1110	9241	9824
11 1111	9340	9951

Note:

OUTDLY[5:0] and ADDR = D, FDDLY[5:0] are for LVDS data OUT8-1, DCLK and FCLK alignment delay time setting.

ADDR=0 D[1:0]

ATP[1:0] LVDS Alignment Test Pattern Control Table

D1	D0	LVDS Output Description
0	0	Latest ADC Results.
0	1	TPDC[11:0] data written in ADDR[C], the LVDS testing data #C.
1	0	Fixed predefined test pattern: "1000 0000 0000"
1	1	TPD1[11:0] data written in ADDR[1], the LVDS testing data #1.

ADDR=2,3,4 or 5 D[5:0] or D[11:6]

CWn Cross-Point Switch Control Table (n=1 to 8 for Ch1 to Ch8)

C5	C4	C3	C2	C1	C0	Description
0	X	X	X	X	X	CW channel Power Down
1	0	X	0	0	0	Differential mode CW1+, CW1-
1	0	X	0	0	1	Differential mode CW2+, CW2-
1	0	X	0	1	0	Differential mode CW3+, CW3-
1	0	X	0	1	1	Differential mode CW4+, CW4-
1	0	X	1	0	0	Differential mode CW5+, CW5-
1	0	X	1	0	1	Differential mode CW6+, CW6-
1	0	X	1	1	0	Differential mode CW7+, CW7-
1	0	X	1	1	1	Differential mode CW8+, CW8-
1	1	0	0	0	0	Single-ended mode CW1+
1	1	0	0	0	1	Single-ended mode CW2+
1	1	0	0	1	0	Single-ended mode CW3+
1	1	0	0	1	1	Single-ended mode CW4+
1	1	0	1	0	0	Single-ended mode CW5+
1	1	0	1	0	1	Single-ended mode CW6+
1	1	0	1	1	0	Single-ended mode CW7+
1	1	0	1	1	1	Single-ended mode CW8+
1	1	1	0	0	0	Single-ended mode CW1-
1	1	1	0	0	1	Single-ended mode CW2-
1	1	1	0	1	0	Single-ended mode CW3-
1	1	1	0	1	1	Single-ended mode CW4-
1	1	1	1	0	0	Single-ended mode CW5-
1	1	1	1	0	1	Single-ended mode CW6-
1	1	1	1	1	0	Single-ended mode CW7-
1	1	1	1	1	1	Single-ended mode CW8-

ADDR=6 D[8]

CW/TGC TGC or CW Mode Control

0	TGC mode. CH[8:1]=1 for TGC (LNA+VGA+AAF) channel 1-8 power down individually.
1	CW mode. MSB (C5) of CWn[5:0] per channel control power down channel individually.

Note:

See CWn Cross-Point Switch Control Table

ADDR=6 D[7:0]

CHOFF[7:0] TGC (LNA+VGA+AAF) Channel Power Control Table

D7	D6	D5	D4	D3	D2	D1	D0
TGC Ch8	TGC Ch7	TGC Ch6	TGC Ch5	TGC Ch4	TGC Ch3	TGC Ch2	TGC Ch1

Note:

0 = ON, 1 = OFF (power down)

ADDR=7 D[9:8]

AAF[1:0] Cutoff Frequency and Control Table

AAF[1:0]	3rd Order Anti-Aliasing Filter Corner Freq fAAF				
	Min	Typ	Max	Units	Note
00	6.6	FS/3	15	MHz	100% as default
01	115			%	% of default
10	Set by AAF[5:2]			MHz	
11	85			%	% of default

ADDR=7 D[6]

PDC Enable External Biasing

0	Disable external Biasing for VGA
1	Enable external Biasing for VGA

ADDR=7 D[5]

FLEX AAF Tracking Auto-Tuning Control

0	FLEX = 0 disable continuous auto-tuning for AAF tracking the input clock.
1	FLEX=1 enable continuous auto-tuning for AAF tracking the input clock,

Note:

FLEX must be set to "1" first then to "0" to turn off the AFF auto-tracking after the chip power on, although the power-on default is FLEX = 0.

ADDR=7 D[3]

SWLNA LNA Gain Switches Control

0	SW1~8 Off, disconnecting R_{f2} to PA- terminal.
1	SWLNA=1 On, connecting R_{f2} to PA- terminal.

ADDR=7 D[2]

GAINLNA LNA Gain Control

0	LNA gain set to 18dB
1	LNA gain set to 14dB

ADDR=7 D[1:0]

PG[1:0] Gain Setting

00	Select 23.5dB Gain Setting
01	Select 29.0dB Gain Setting
10	Select 34.5dB Gain Setting
11	Select 40.0dB Gain Setting

ADDR=8 D[9]

CTL AAF Frequency Programming Enable

0	AAF use AAF[5:2] tracking the sampling frequency.
1	AAF use PR[5:2] programmed frequency.

Note:

See AAF and PR tables

ADDR=8 D[8:5]

PR[5:2] Cutoff Frequency Direct Control Table (CTL = 1)

PR[5:2]	Reference -3dB Cut-off Frequency (MHz)	Note
0000	15.8	Max. built-in AAF frequency
0001	14.3	
0010	12.9	
0011	11.8	
0100	10.8	
0101	9.9	
0110	9.2	
0111	8.6	
1000	8.0	
1001	7.6	
1010	7.1	
1011	6.8	
1100	6.4	
1101	6.0	
1110	5.8	
1111	5.6	Min. built-in AAF frequency

ADDR=8 D[3:0]

AAF[5:2] Cutoff Frequency Control Table (AAF[1:0]=10)

SPI Control Register Data Bits				Typical -3dB Cut-off Frequency (MHz)			
AAF5	AAF4	AAF3	AAF2	F_S = 50MHz	F_S = 40MHz	F_S = 30MHz	F_S = 20MHz
1	1	1	1	15.6	12.5	9.5	6.1
1	1	1	0	13.4	10.7	8.7	5.9
1	1	0	1	12.8	10.2	8.1	5.8
1	1	0	0	11.9	9.5	7.6	5.8
1	0	1	1	10.9	8.7	7.0	5.8
1	0	1	0	10.0	8.1	6.7	5.8
1	0	0	1	9.5	7.6	6.2	5.8
1	0	0	0	8.8	7.0	6.0	5.8

ADDR=9 D[7:0]

ADCPD[7:0] ADC Channel Power down Control Table

D7	D6	D5	D4	D3	D2	D1	D0
ADC Ch8	ADC Ch7	ADC Ch6	ADC Ch5	ADC Ch4	ADC Ch3	ADC Ch2	ADC Ch1

Note:

0 = ON, 1 = OFF (power down)

ADDR=B D[11:9]

SWING[2:0] LVDS Output Swing Control Table

SWING[2:0]	LVDS Output Swing Amplitude (mV)
000	350 (Default value)
001	263
010	175
011	88
100	700
101	613
110	525
111	438

ADDR=D D[11:6]

FDDLY[5:0] LVDS FCLK & DCLK Delay Adjustment Table

FDDLY[5:0]	Typical Rise Time Delay (ps)	Typical Fall Time Delay (ps)
00 0000	655	685
00 0001	766	805
… …	DELAY = 139.4 x FDDLY + 655	DELAY = 148.5 x FDDLY + 699
11 1110	9241	9824
11 1111	9340	9951

Note:

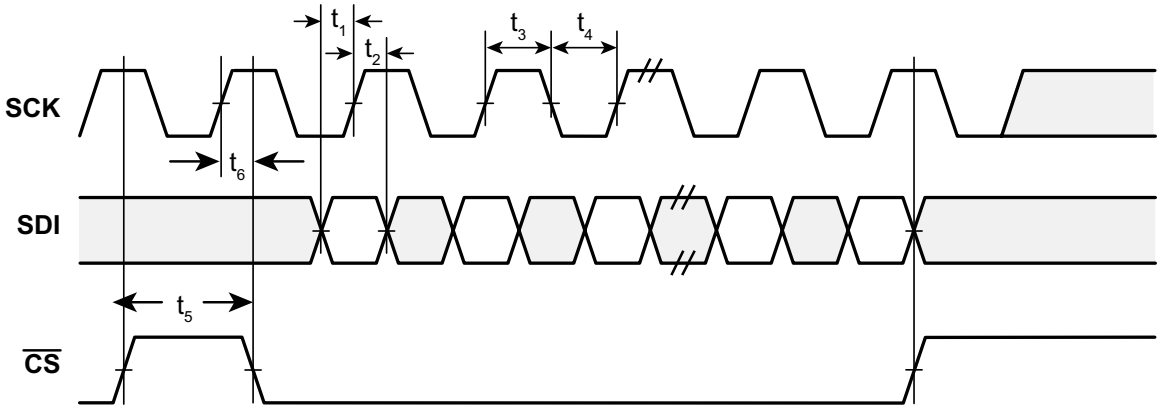
OUTDLY[5:0] and ADDR=D, FDDLY[5:0] are for LVDS data OUT8-1, DCLK and FCLK alignment delay time setting.

ADDR=F D[11:8]

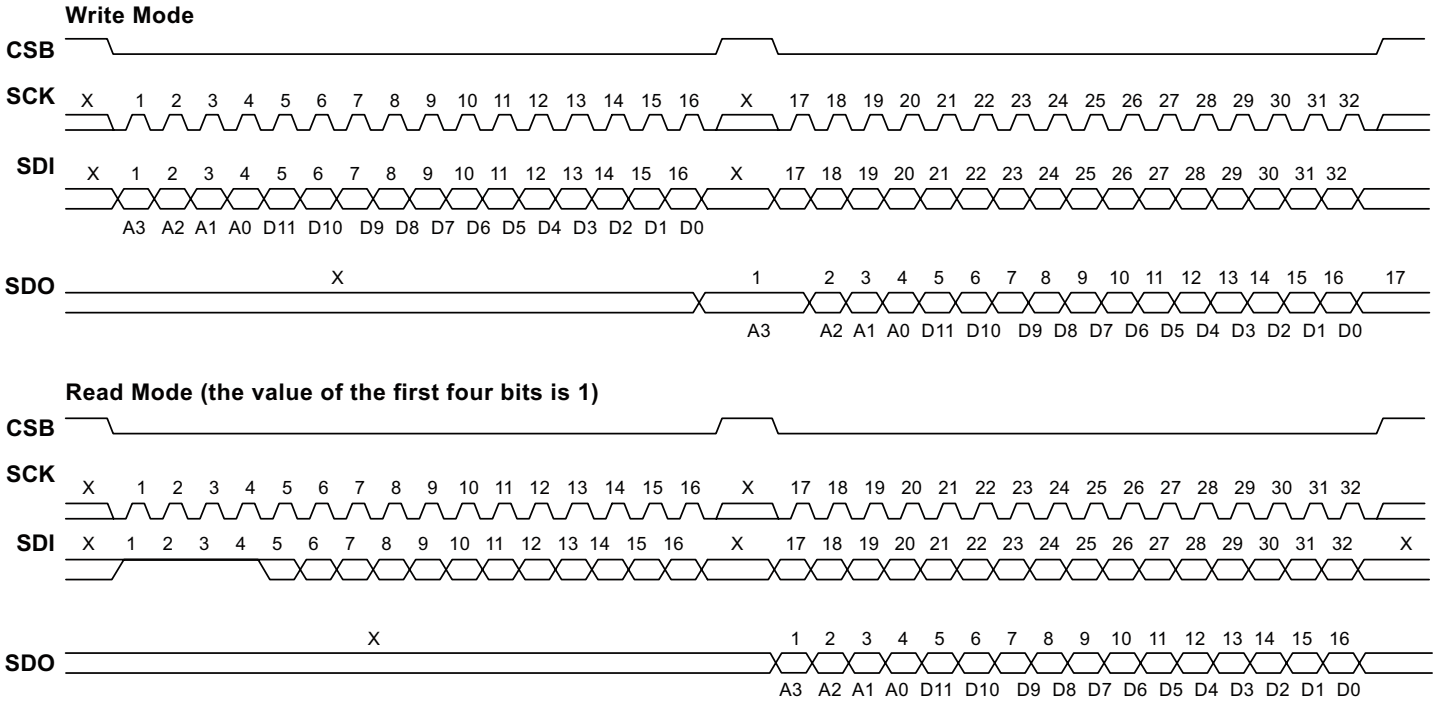
ADDR[3:0] Register Contain Read Back Address

0000	Read Back Register ADDR = 0x0
0001	Read Back Register ADDR = 0x1
…	…
1110	Read Back Register ADDR = 0xE

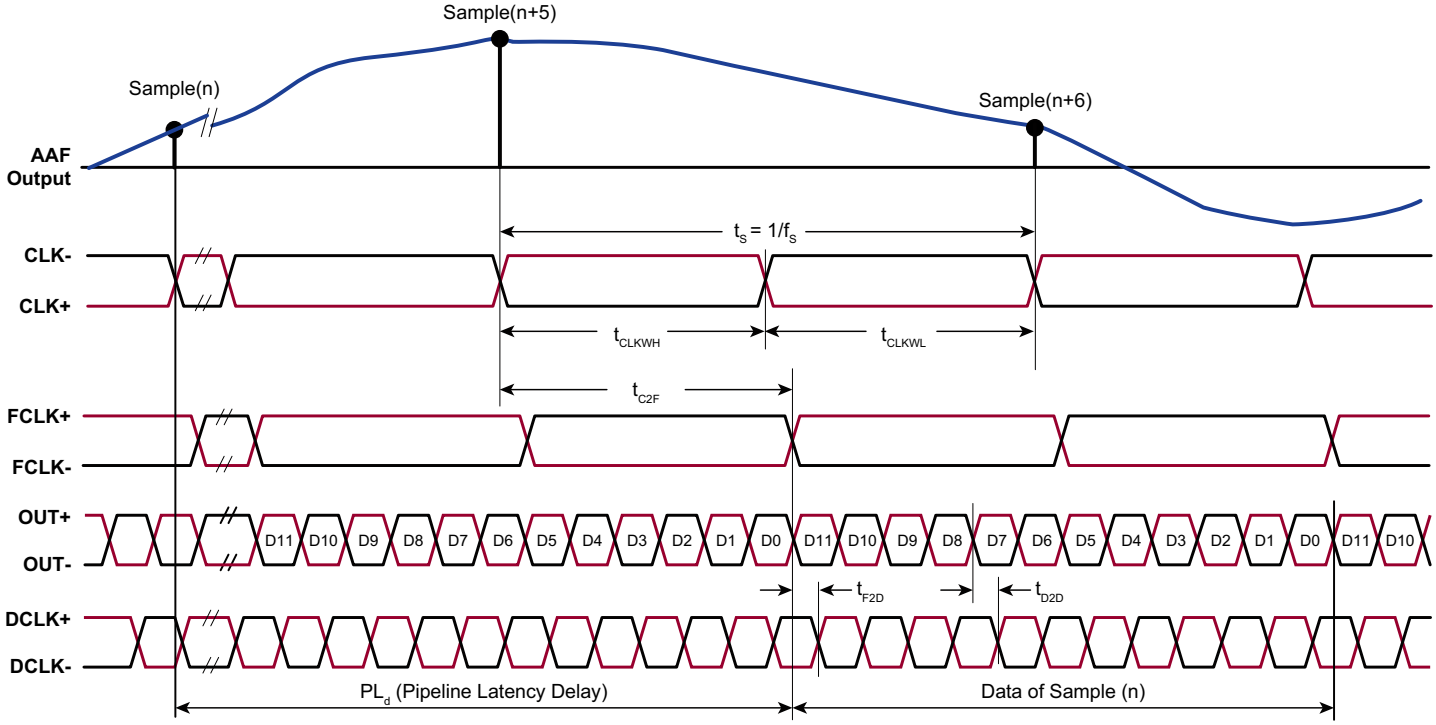
SPI Timing Diagram



SPI Data Diagram



LVDS Timing Diagram



General Description

The MD3872 has eight identical front-end receiver channels designed for medical ultrasound imaging. Each channel consists of a low noise preamplifier (LNA), a variable gain amplifier (VGA), an anti-aliasing filter (AAF), and a 12-bit analog-to-digital converter (ADC). The VGA consists of two parts, a voltage controlled attenuator (VCA), and a programmable gain amplifier (PGA). The gain and gain range of the VGA can be digitally configured separately. The gain of the LNA is selectable. The differential outputs of each LNA can also be used to provide amplified RF signals for the CW Doppler beamforming processing. The voltage-controlled-gain TGC attenuator can be continuously varied by a control voltage at the TGC pin from -47dB to a maximum of 0dB. The gain of the TGC curve is linear-in-dB, and the slope of the curve can be adjusted by the input voltage of GSC pin for all the eight channels in the same chip.

The TGC attenuator output is AC-coupled into the PGA. PGA gain is programmed through the two gain bits (PG0 and PG1) in the SPI control register, and can be configured to four different gain settings of 23.5, 29, 34.5 and 40dB.

The AAF is a third-order Butterworth low-pass filter. The auto-tracking cutoff frequency is typically one-third of the sampling frequency, and is typically triggered by the FLEX command calibration. There are control bits in SPI for adjusting the auto-tracking cutoff frequency up to ±15% of the typical value for the anti-aliasing filter. In addition, the SPI control register AAF bits can set more frequency range options.

The ADC converters in the MD3872 use a very low power, high-speed, self-calibrated pipeline architecture that moves the samples through the pipeline stages every half clock-cycle. The converted digital results are serialized and sent through the LVDS output drivers. The total latency is 5.5 input clock cycles.

The following sections are detail descriptions of each programmable feature.

LNA Gain & Active Impedance Matching

The LNA consists of a differential voltage gain low noise amplifier. The LNA's inverting single-ended output gain is A = 4.0 and A = 2.5 when the LNA differential gain is 18dB and 14dB, respectively. With a known fixed gain, a feedback resistor can be connected between the LNA positive input pin (IN1+) and the inverting output pin (PA1-), and in series with a capacitor. This technique is well known as active termination and results in a better noise figure (NF) than passive termination. The effective input resistance is RIN = RFB/(1+A). In addition, the MD3872 provides a dual mode feedback resistor option for connecting two feedback resistors in parallel through the SWx pins. The SWx pin is connected to the PAx pin with an internal switch which is controlled by the SWLNA bit in SPI.

TGC / CW Mode & Power Consumption

At power up, all the SPI register's data bits are reset to 0, and the MD3872 will go into the default: all TGC mode and the whole chip's current consumption is approximately 760mW if the sampling clock is 40MHz. When in the default state, CW/$\overline{\text{TGC}}$ = 0, (ADDR=6, D[7:0]='00000000'), ADCPD[7:0] ='00000000', all channels of LNA, VGA, AAF and ADC are turned on. At the same time, PLL and LVDS will be turned on in this mode.

To control each TGC (LNA+VGA+AAF) channel individually, ADDR = 6, CHOFF[7:0] provides selection of turning ON/OFF for each TGC channel. For example, when MD3872 is in TGC mode, CW/$\overline{\text{TGC}}$ = 0 and CHOFF[7:0] = '01111111', only the TGC channel 8 is switched ON and other channels are switched OFF. In this condition, the whole chip's current consumption will be quite a bit less than when all channels are ON. To power off each ADC individually in TGC mode, ADDR = 9, ADCPD[7:0] can be programmed to state1. For example, ADCPD[7:0] = '10000000', ADC8 is powered down and the others are powered on. Note that in TGC mode, ADDR = 2, 3, 4 and 5 are meaningless.

If CW/$\overline{\text{TGC}}$ = 1, MD3872 will go into CW mode, all the VGA, ADC, AFF, LVDS and PLL will be shut down automatically and ADDR = 6, D[7:0] is meaningless. In CW mode, each channel's CW trans-conductance amplifiers ON and OFF are controlled by ADDR = 2,3,4 and 5 as shown in the CW cross-point switch control register table. For example, if CW/$\overline{\text{TGC}}$ = 1, ADDR 2, D[11:0] ='100000100000', the MD3872 will be in CW mode and CW channels 1 and 2 will be turned on. At that time, LNA1 and LNA2 and CW-SW circuits will turn on, and the total CW output current coming from the channel 1 and channel 2 trans-conductance amplifiers will be differentially mixed into CW1+ and CW1-. The VDD current is about 25mA increasing per CW channel. If setting ADDR = 2 to 5 to CW mode ON state, all the LNA and CW trans-conductance amplifiers are switched ON.

Anti-Aliasing Filter

The MD3872 provides two options for setting the AAF corner frequency in TGC mode. The first option is the sampling frequency tracking method in which the corner frequency is tracked with 1/3 of the sampling frequency. It is achieved by the built-in six-bit resolution programmable RC value analog anti-aliasing filter for tracking with sampling frequency, temperature and process corner. It is enabled by CTL = 0 and

FLEX bit/pin. The second option is the direct control method in which the corner frequency is set by directly programming the first four bits of the six-bit resolution. It is enabled by CTL = 1. However, in this mode, the corner frequency is not tracked with temperature and process. The tolerance can be up to +/- 20% . It is the easier method, as there is no need to trigger the FLEX pin/bit periodically. The direct control method is recommended if the application can tolerate a higher variation of the TGC bandwidth.

In sampling frequency tracking mode (CTL = 0), the ADDR = 7, D5 is FLEX to control the built-in AAF auto-tracking function. It is used only in TGC mode in which the AAF circuit is in operation. This SPI bit has the same function as the external FLEX pin. Either setting the SPI FLEX bit or setting the external pin can enable the AAF auto-tracking operation. If FLEX = 1, the auto-tracking circuit will function and the AAF corner frequency will track with the external sampling clock. The tacking lock-in process time is less than 50µs. The tracking program will keep on generating a new six-bit code in each cycle for all the analog filters. Thus, it needs to set FLEX back to 0 if the programming operation is completed for the whole ultrasound system, otherwise, it will generate extra noise for the chip, and therefore precautions need to be applied. Before enabling this mode, the ADDR = 7, AAF[1:0] and ADDR = 8, AAF[5:2] should be programmed first. The default state of AAF[1:0] sets the resultant tracking value to 100% of the 1/3 of the sampling frequency. As in some applications, it may need a around 15% higher or 15% lower of the 1/3 of the sampling frequency value or another more precise offset lower value (controlled by AAF[5:2]) with respect to the 1/3 sampling frequency to achieve an appropriate TGC bandwidth for better noise performance. The AAF[5:0] control bits descriptions are shown in the AAF control table.

In the direct control method (CTL = 1), ADDR = 8, D[8:5] is PR[5:2] to directly program the code for setting the AAF corner frequency as shown in the cut-off frequency direct control table. For example, if the signal tone is 3.0MHz and the application needs the lowest AAF corner frequency for the lowest noise bandwidth such that the SNR will be the highest, the PR[5:2] should be set to ‘1111’.

The ADDR = 7, D3 and D2 are SWLNA and GAINLNA to control the LNA feedback resistor switch and LNA gain as shown in data sheet SPI register table’s notes-6 and -7. These bits will affect both TGC mode and CW mode. The feedback resistor switch option is for re-matching the input impendence externally if the LNA gain is changed. The ADDR = 7, D1 and D0 are PG[1:0] for the gain settings of VGA.

ADC Clock and PLL

ADC is the eight-channel analog to digital converter and is driven by the ADC sampling-frequency clock CLK+/CLK- LVDS input pair which normally operates from a low-jitter external 20 to 40MHz LVDS clock source. The built-in PLL phase-locked loop circuit will provide six times the input frequency as the DCLK serial data bit clock and a phase shifted version with the same frequency as the FCLK data-frame clock. The PLL also provides the ADC internal switching and conversion clocks. It is highly recommended routing the CLK+/CLK- input trace as a well controlled impedance differential LVDS line-pair, with a 100Ω resistor as termination resistor right at the device CLK pins.

LVDS Data Alignment Pattern

There are two 12-bit digital output test binary pattern registers TPD1[11:0] and TPDC[11:0] available that can be programmed through the SPI. The SPI control register bit ATP[1:0] selects which pattern or data of ADC results to provide to the LVDS data output. These patterns allow the user to perform timing alignment adjustments among the ADCLK and LCLK, and output data.

LVDS Outputs and Clock Timing & Delay Adjustment

The differential outputs conform to a low power, reduced signal option of the ANSI-644 standard. The LVDS outputs are designed for interfacing with LVDS receivers in custom ASICs or FPGAs that have LVDS capability up to 480 MB/sec with a 100Ω termination resistor placed as close to the receiver as possible. It is recommended that the trace length be no longer than 12 inches and that the differential output traces be kept close together and at equal lengths.

The format of the output data is offset binary by default. An example of the output coding format can be found in the table above. Two output clocks are provided to assist in capturing data from the MD3872. DCLK± is used to clock the output data and is equal to six times the sampling clock rate. Data is clocked out of the MD3872 and must be captured on the rising and falling edges of the CLK± that supports double data rate (DDR) capturing. The frame clock output, CLK± is used to signal the start of a new output byte and is equal to the sampling clock rate. In addition, MD3872 provides LVDS ADC data OUT, FCLK and DCLK output time-delay and swing amplitude adjustment bits in SPI registers OUTDLY, FDDLY, SETP and SWING. For detailed timing, see the timing diagram and tables above.

CW Cross-point Switch and Control

MD3872 consists of an 8x8 CW cross-point switch matrix. There are eight differential inputs and eight differential outputs in the matrix. The differential inputs come from the outputs of a differential transconductance amplifier which is driven by the LNA directly. There are 16 output pins for the eight differential outputs. The outputs of the transconductance amplifier are current outputs, which can be easily routed via switches and perform summing operations for the CWD beamforming function. In single-end mode, only non-inverting transconductance amplifier output current is switched to the selected CW single-ended output. Inverting transconductance amplifier output current is disabled in this mode. All the cross-point switches in the CW switch matrix can be programmed individually through the SPI control interface. The whole CW mode operation occupies four registers in the SPI interface registers map.

Power-Down Mode

The ADDR = 7, D6 is the PDC bit to control where the LNA, CW-SW, VGA, AFF programmable reference current originates. If PDC = 0, the current usage of all four front-end circuits will be referenced from the internal front-end circuit current reference. Note that this circuit will not affect the current usage of PLL, ADC and LVDS circuit. If PDC = 1, the front-end circuits will refer to the external resistor current. In normal operation, it is strongly recommended that the internal reference be used, as it is optimized for the balance of front-end circuits' performance and power consumption. If a 10% reduction in current is desired, set PDC = 1 and connect an external bias resistor from EBC to GND. This will sacrifice a certain amount of performance.Thus, if PDC = 1 and no external resistor is connected to the EBC pin (N.C.), the total current consumption will be decreased to almost no referenced current state.

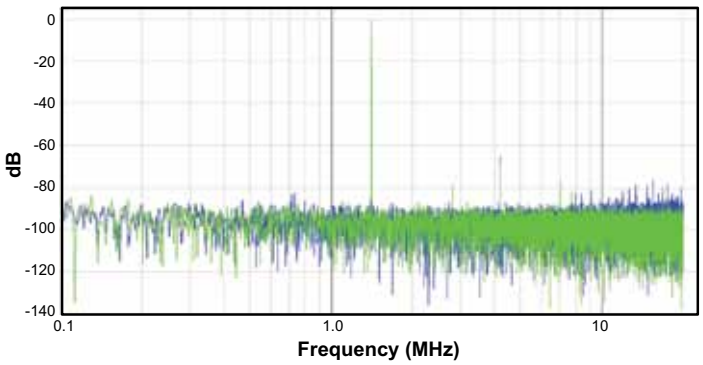


Fig. 1. MD3872 vs Competitor @1.4MHz

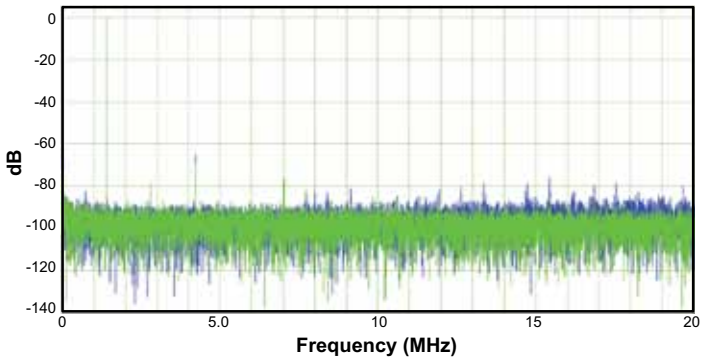


Fig. 2. MD3872 vs Competitor @1.4MHz

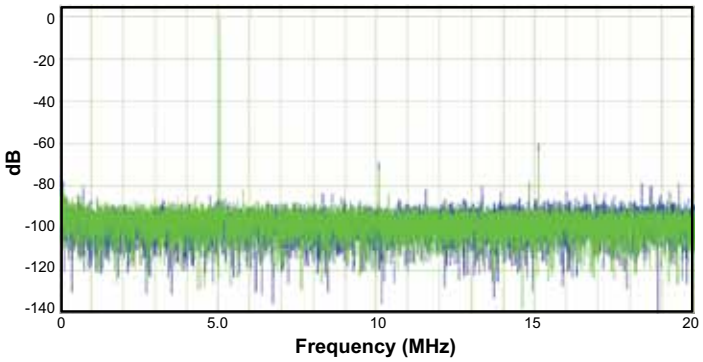


Fig. 3. MD3872 vs Competitor @5.0MHz

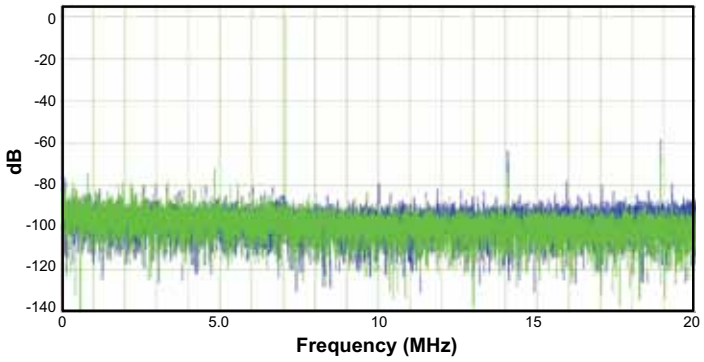


Fig. 4. MD3872 vs Competitor @7.0MHz

Note:

Green: sine wave input to MD3872 on the evaluation board
Blue: some sine wave input to competitor on the evaluation board
Both at f_S = 40MHz, LNA RFB = 250Ω, Gain = 18dB, AAF = 1/3f_S
Sample data length 32768 points FFT with Blackman-Harris Windowing

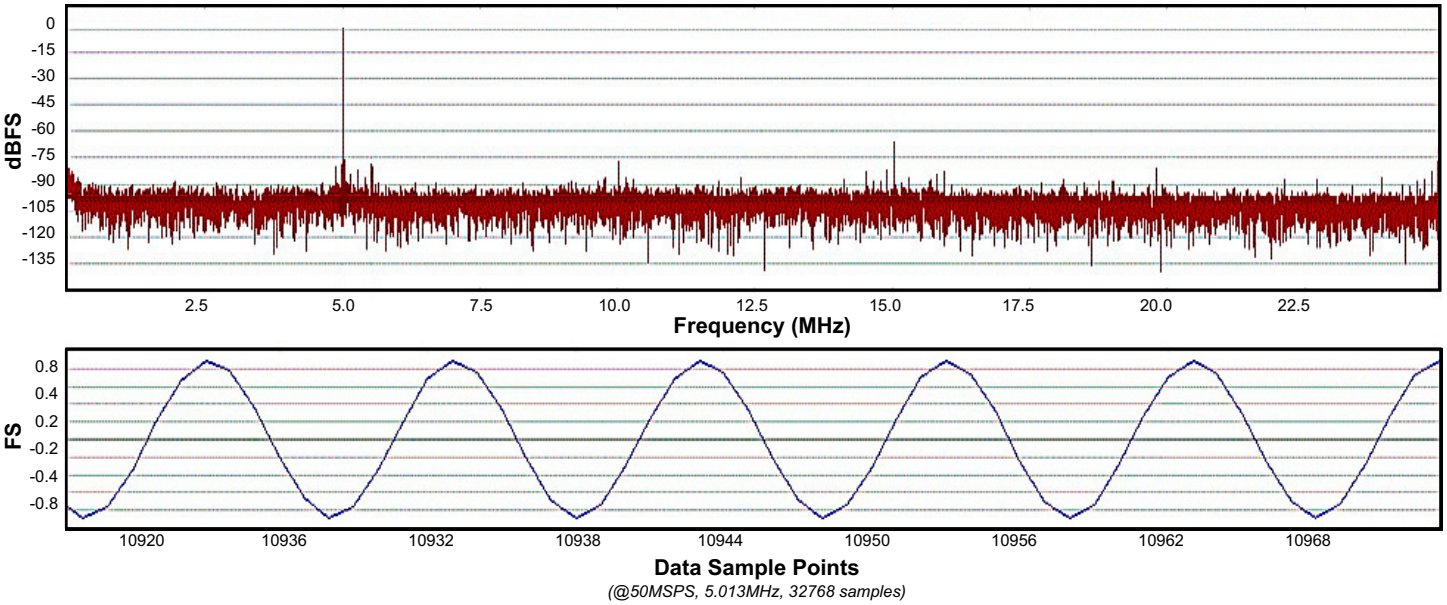


Fig. 5 ADC Output Data Waveform and FFT

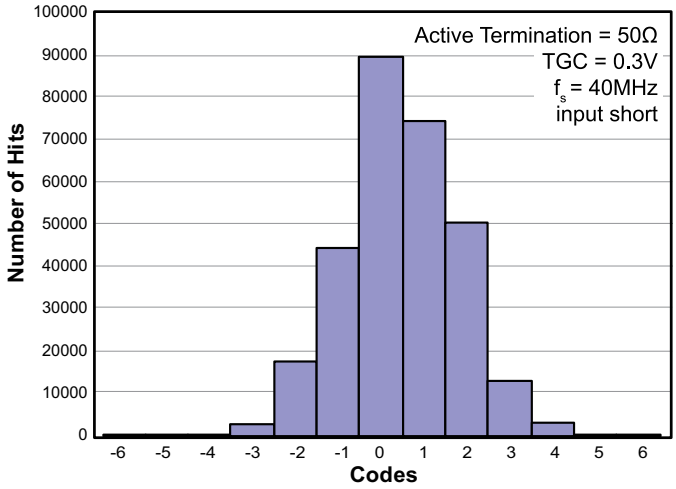


Fig. 6. Output-Referred Noise Histogram (with TGC = 0.3V)

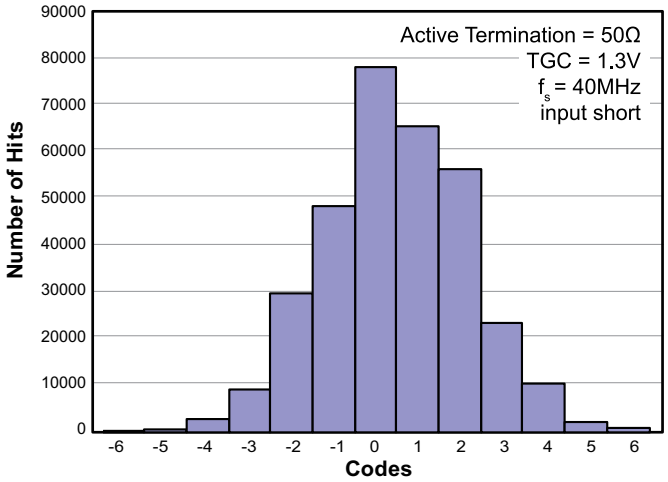


Fig. 7. Output-Referred Noise Histogram (with TGC = 1.3V)

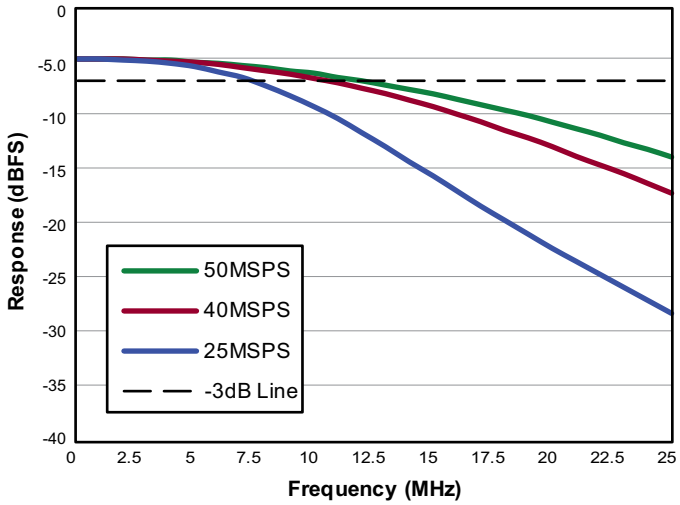


Fig. 8. Antialiasing Filter (AAF) Pass-Band Response, No HPF Applied

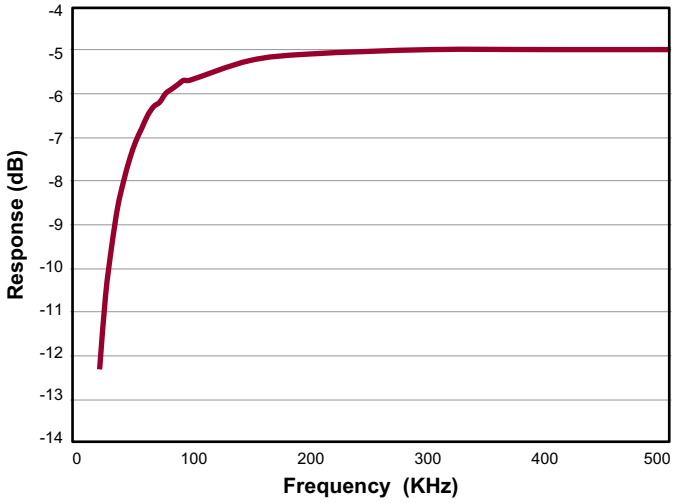


Fig. 9. Channel High-Pass Filter (HPF) Corner Frequency Response

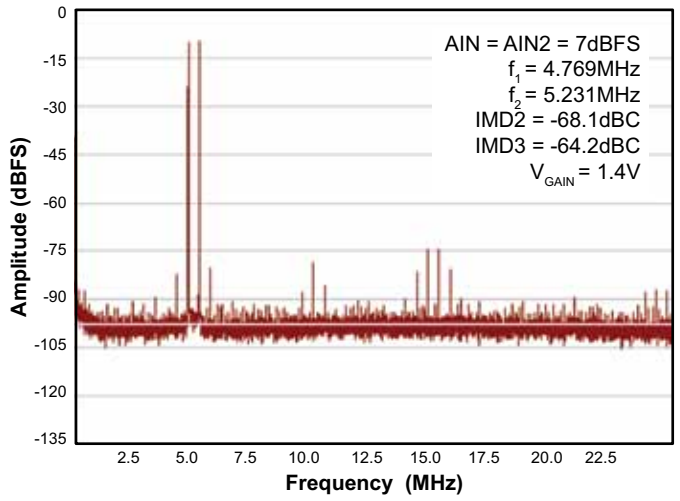


Fig. 10. Typical IMD2 and IMD3 Performance

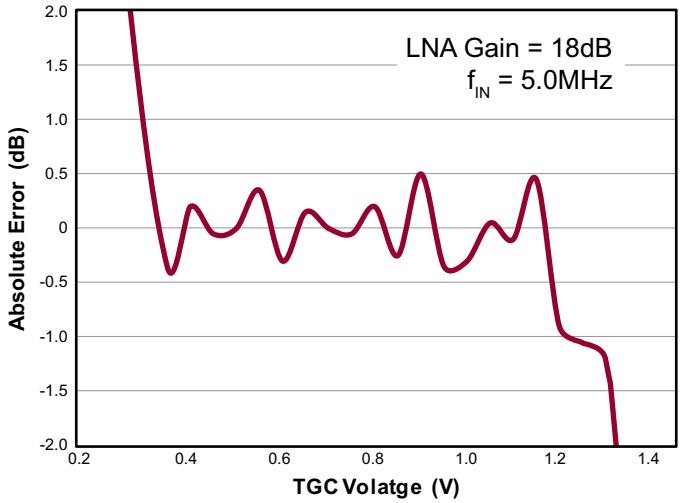


Fig. 11. Gain Error vs. TGC Voltage
(at 25°C @ fs=50MHz, AAF fs/3)

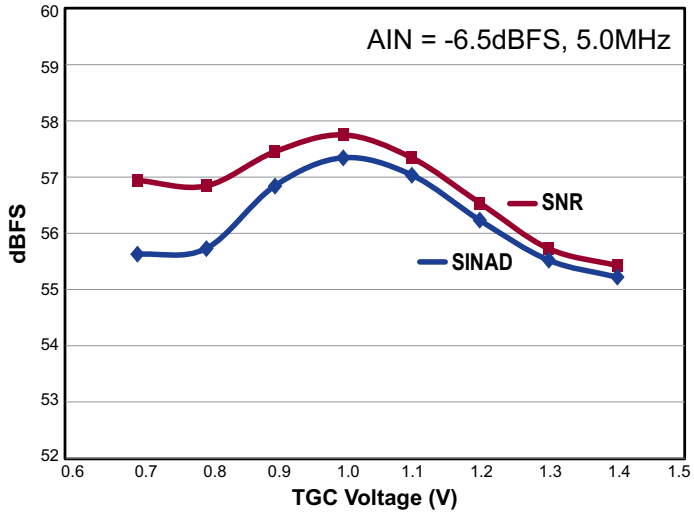


Fig. 12. SNR and SINAD vs. TGC Volatge

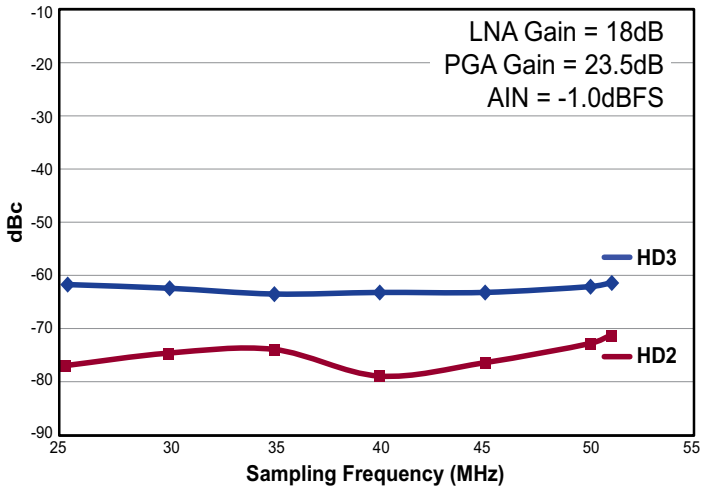


Fig. 13. HD2 & HD3 vs. Sampling Frequency

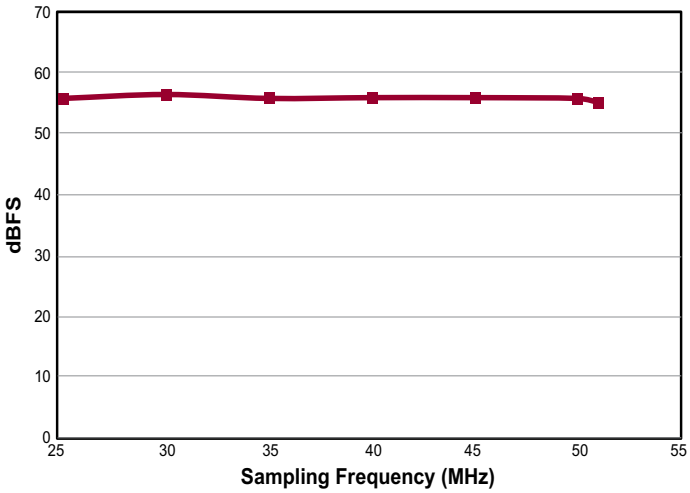


Fig. 14. SNRFS vs. Sampling Frequency

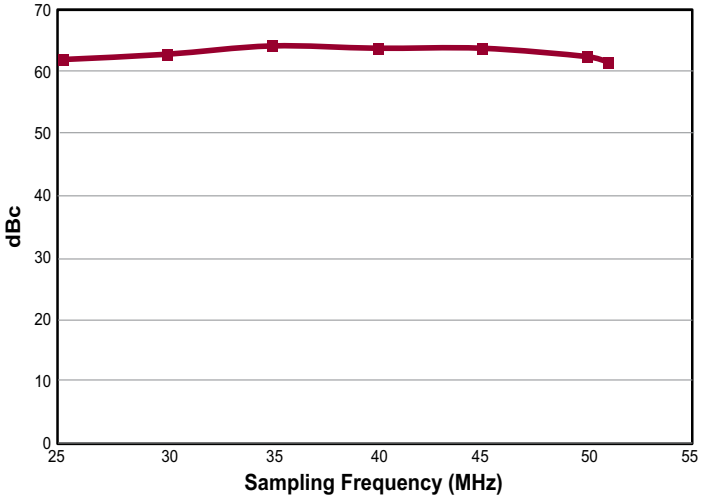


Fig. 15. SFDR vs. Sampling Frequency

Equivalent Circuits

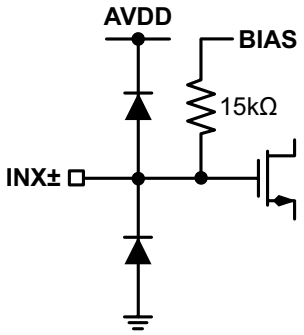


Fig. 16 Equivalent LNA Input Circuit

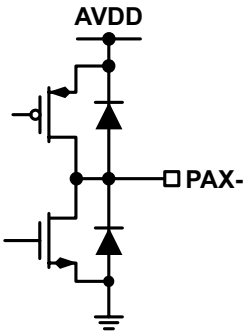


Fig. 17 Equivalent LNA Output Circuit

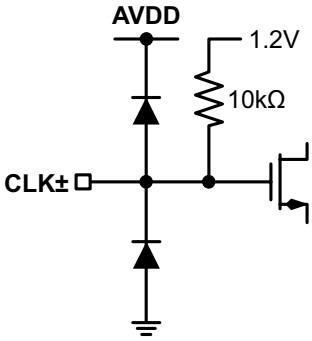


Fig. 18 Equivalent Clock Input Circuit

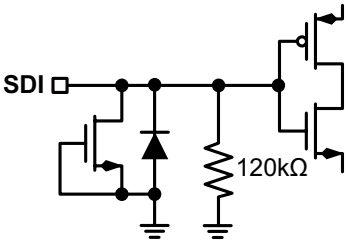


Fig. 19 Equivalent SDI Output Circuit

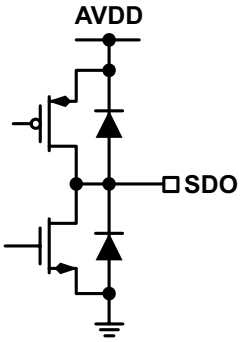


Fig. 20 Equivalent SDO Output Circuit

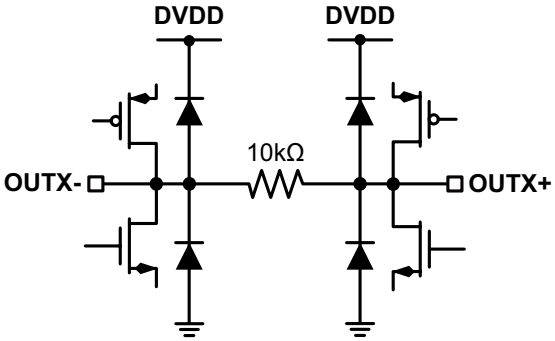


Fig. 21 Equivalent Digital Output Circuit

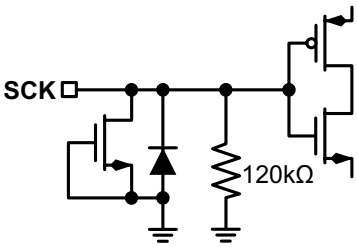


Fig. 22 Equivalent SCK Input Circuit

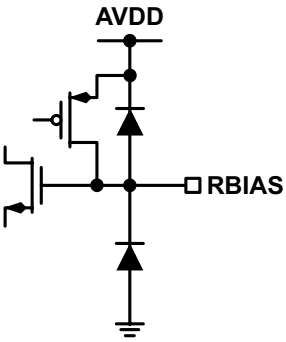


Fig. 23 Equivalent RBIAS Circuit

Equivalent Circuits *(cont.)*

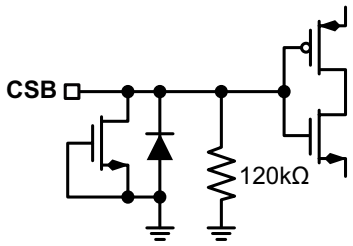


Fig. 24 Equivalent CSB Input Circuit

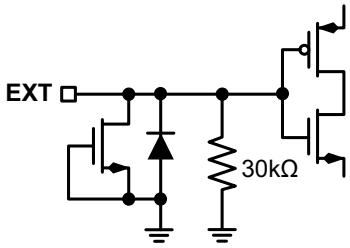


Fig. 25 Equivalent EXT Input Circuit

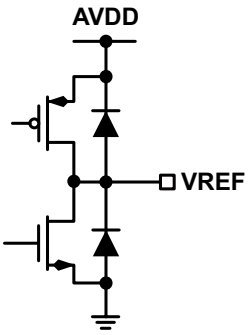


Fig. 26 Equivalent VREF Circuit

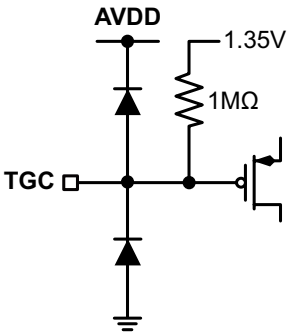


Fig. 27 Equivalent TGC Input Circuit

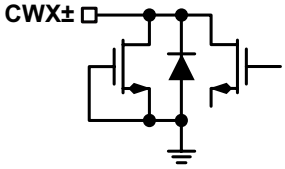


Fig. 28 Equivalent CW Output Circuit

Pin Description

Pin	Designator	Description
1	GND	Ground
2	AVDD2	Supply for ADC (1.8V)
3	AVDD1	Supply for LNA & VGA (1.8V)
4	SW5	Channel 5 LNA Output Complement
5	PA5-	Channel 5 LNA Negative Output
6	IN5+	Input Channel 5
7	CM5	Channel 5 Common-mode decoupling, bypass to ground
8	IN5-	Complementary Input Channel 5
9	AVDD2	Supply for ADC (1.8V)
10	AVDD1	Supply for LNA & VGA (1.8V)
11	SW6	Channel 6 LNA Output Complement
12	PA6-	Channel 6 LNA Negative Output
13	IN6+	Input Channel 6
14	CM6	Channel 6 Common-mode decoupling, bypass to ground
15	IN6-	Complementary Input Channel 6
16	AVDD2	Supply for ADC (1.8V)
17	AVDD1	Supply for LNA & VGA (1.8V)
18	SW7	Channel 7 LNA Output Complement
19	PA7-	Channel 7 LNA Negative Output
20	IN7+	Input Channel 7
21	CM7	Channel 7 Common-mode decoupling, bypass to ground
22	IN7-	Complementary Input Channel 7
23	AVDD2	Supply for ADC (1.8V)
24	AVDD1	Supply for LNA & VGA (1.8V)
25	SW8	Channel 8 LNA Output Complement
26	PA8-	Channel 8 LNA Negative Output
27	IN8+	Input Channel 8
28	CM8	Channel 8 Common-mode decoupling, bypass to ground
29	IN8-	Complementary Input Channel 8
30	GND	Ground
31	CLK-	Negative clock input pin
32	CLK+	Positive clock input pin
33	AVDD4	Supply for Clock distribution circuit (1.8V)
34	SDO	Serial Data Output

Pin Description *(cont.)*

Pin	Designator	Description
35	NC	Reserved, do not connect
36	AVDD5	Supply for PLL (1.8V)
37	DVDD	Supply for LVDS (1.8V)
38	OUT8-	ADC LVDS output negative - Channel 8
39	OUT8+	ADC LVDS output positive - Channel 8
40	OUT7-	ADC LVDS output negative - Channel 7
41	OUT7+	ADC LVDS output positive - Channel 7
42	OUT6-	ADC LVDS output negative - Channel 6
43	OUT6+	ADC LVDS output positive - Channel 6
44	OUT5-	ADC LVDS output negative - Channel 5
45	OUT5+	ADC LVDS output positive - Channel 5
46	FCLK-	Negative LVDS frame clock output
47	FCLK+	Positive LVDS frame clock output
48	DCLK-	Negative LVDS data clock
49	DCLK+	Positive LVDS data clock
50	OUT4-	ADC LVDS output negative - Channel 4
51	OUT4+	ADC LVDS output positive - Channel 4
52	OUT3-	ADC LVDS output negative - Channel 3
53	OUT3+	ADC LVDS output positive - Channel 3
54	OUT2-	ADC LVDS output negative - Channel 2
55	OUT2+	ADC LVDS output positive - Channel 2
56	OUT1-	ADC LVDS output negative - Channel 1
57	OUT1+	ADC LVDS output positive - Channel 1
58	DVDD	Supply for LVDS (1.8V)
59	N.C	Reserved, do not connect
60	STBY	Standby
61	PDWN	Power down
62	AVDD6	Supply for SPI (1.8V)
63	SCLK	Serial clock
64	SDI	Serial data input
65	CSB	Chip select bar
66	NC	Reserved, do not connect
67	NC	Reserved, do not connect
68	IN1-	Complementary Input Channel 1

Pin Description *(cont.)*

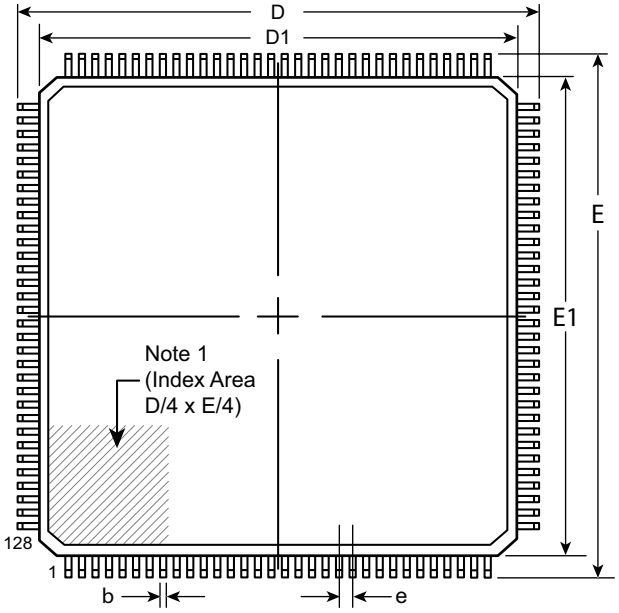
Pin	Designator	Description
69	CM1	Channel 1 Common-mode decoupling, bypass to ground
70	IN1+	Input Channel 1
71	PA1-	Channel 1 LNA Negative Output
72	SW1	Channel 1 LNA Output Complement
73	AVDD1	Supply for LNA & VGA (1.8V)
74	AVDD2	Supply for ADC (1.8V)
75	IN2-	Complementary Input Channel 2
76	CM2	Channel 2 Common-mode decoupling, bypass to ground
77	IN2+	Input Channel 2
78	PA2-	Channel 2 LNA Negative Output
79	SW2	Channel 2 LNA Output Complement
80	AVDD1	Supply for LNA & VGA (1.8V)
81	AVDD2	Supply for ADC (1.8V)
82	IN3-	Complementary Input Channel 3
83	CM3	Channel 3 Common-mode decoupling, bypass to ground
84	IN3+	Input Channel 3
85	PA3-	Channel 3 LNA Negative Output
86	SW3	Channel 3 LNA Output Complement
87	AVDD1	Supply for LNA & VGA (1.8V)
88	AVDD2	Supply for ADC (1.8V)
89	IN4-	Complementary Input Channel 4
90	CM4	Channel 4 Common-mode decoupling, bypass to ground
91	IN4+	Input Channel 4
92	PA4-	Channel 4 LNA Negative Output
93	SW4	Channel 4 LNA Output Complement
94	AVDD1	Supply for LNA & VGA (1.8V)
95	AVDD2	Supply for ADC (1.8V)
96	GND	Ground
97	GND	Ground
98	FLEX	Enable automatic low-pass tuning 1 = on, 0 = off (default)
99	AVDD7	Supply for auto-tuning circuit (1.8V)
100	CW1+	CW Switch Output
101	CW1-	CW Switch Output
102	CW2+	CW Switch Output

Pin Description *(cont.)*

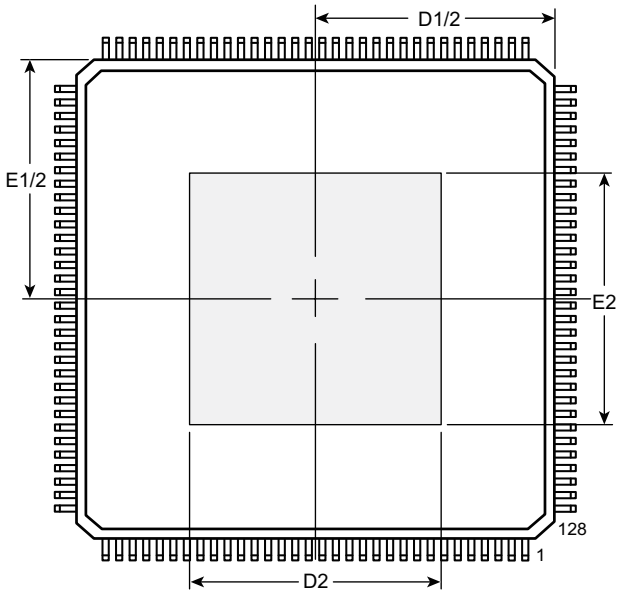
Pin	Designator	Description
103	CW2-	CW Switch Output
104	CW3+	CW Switch Output
105	CW3-	CW Switch Output
106	CW4+	CW Switch Output
107	CW4-	CW Switch Output
108	CVDD	CW VDD (3.3V)
109	RBIAS	Bias Setting Resistor (50kΩ to GND)
110	EXT	Internal/external reference select, Hi = External reference is selected
111	VREF	Supply (1.0V)
112	REF-	Differential reference (-), external decoupling capacitors 0.1μF//10μF to REF+, and 0.1μF to GND
113	REF+	Differential reference (+), external decoupling capacitors 0.1μF//10μF to REF-, and 0.1μF to GND
114	AVDD3	Supply for ADC reference circuit (1.8V)
115	CVDD	CW VDD 3.3V
116	CW5+	CW Switch Output
117	CW5-	CW Switch Output
118	CW6+	CW Switch Output
119	CW6-	CW Switch Output
120	CW7+	CW Switch Output
121	CW7-	CW Switch Output
122	CW8+	CW Switch Output
123	CW8-	CW Switch Output
124	AVDD0	Supply for LNA & VGA bias (1.8V)
125	TGC	TGC attenuator control input for all channel, 0 to 1.8V
126	GSC	TGC optional slope adjustment voltage input.
127	CM0	Common-mode decoupling, bypass to ground
128	EBC	External Current Bias, Do not connect
Thermal Slug	GND	Thermal Slug must externally connect to the RF ground and PCB heat sink

128-Lead TQFP (w/Heat Slug) Package Outline (HF)

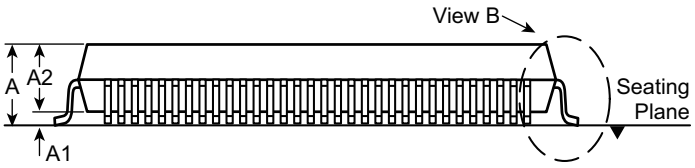
14.00x14.00mm body, 1.20mm height (max), 0.40mm pitch



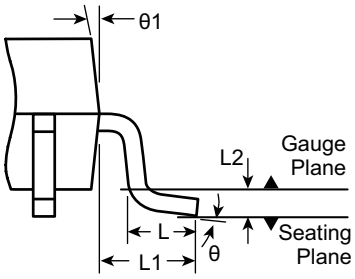
Top View



Bottom View



Side View



View B

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	D2	E	E1	E2	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	-	0.05	0.95	0.13	16.00 BSC	14.00 BSC	9.50 BSC	16.00 BSC	14.00 BSC	9.50 BSC	0.40 BSC	0.45	1.00 REF	0.25 BSC	0°	11°
	NOM	-	-	1.00	0.18								0.60			3.5°	12°
	MAX	1.20	0.15	1.05	0.23								0.75			7°	13°

Drawings not to scale.
Supertex Doc. #: *DSPD-128TQFPHF, Version NR011713.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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